



**SETHU INSTITUTE OF TECHNOLOGY  
PULLOOR, KARIAPATTI – 626 115**



**21UEC404 LINEAR INTEGRATED CIRCUITS**

21UEC404	LINEAR INTEGRATED CIRCUITS	L	T	P	C
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<b>OBJECTIVES:</b>					
<ul style="list-style-type: none"> <li>● To impart knowledge in basic building blocks of linear integrated circuits</li> <li>● To make the students to learn the linear and non-linear applications of operational amplifiers</li> <li>● To familiarize some special function ICs</li> <li>● To prepare the students to learn the types of ADC and DAC</li> </ul>					
<b>UNIT 1</b>	<b>BASICS OF OPERATIONAL AMPLIFIERS</b>	<b>2 0</b>			
<p>Current sources, Voltage sources, Basic information about op-amps — Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations with different input configurations. Applications of op-amps.</p> <ol style="list-style-type: none"> <li>1. Inverting, Non inverting and differential amplifiers.</li> <li>2. Integrator and Differentiator.</li> <li>3. Instrumentation amplifier</li> </ol>					
<b>UNIT 2</b>	<b>OPERATIONAL AMPLIFIERS APPLICATIONS AND SPECIAL FUNCTION ICs</b>	<b>2 5</b>			
<p>Sign Changer, Scale Changer, Phase Shift Circuits, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, peak detector, clipper and clamper, filters, Sine-wave generators, Multivibrators ,Saw-tooth wave generator, ICL8038 Function generator, Timer IC 555, IC Voltage regulators. Applications of Voltage regulators</p> <ol style="list-style-type: none"> <li>1. Active low-pass and band-pass filters.</li> <li>2. Schmitt Trigger using op-amp.</li> <li>3. Phase shift and Wien bridge oscillators using Op-amp.</li> <li>4. Astable and Monostable multivibrators using NE555 Timer.</li> </ol>					
<b>UNIT 3</b>	<b>DATA CONVERTERS</b>	<b>2 5</b>			
<p>Analog and Digital Data Conversions, D/A converter — specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R - 2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type — Dual Slope type. Applications of data convertors.</p> <ol style="list-style-type: none"> <li>1. R-2R Ladder Type D- A Converter using Op-amp.</li> <li>2. Study of SMPS simulation using SPICE: Filters using Op-amp</li> <li>3. Multivibrators using NE555 Timer.</li> </ol>					
<b>TOTAL : 70 PERIODS</b>					

## COURSE OUTCOMES

After completion, the student will be able to

**CO1** Describe the concepts of linear integrated circuits (Understand)

**CO2** Design the linear and nonlinear applications of an Op- Amp along with special function ICs (Apply)

**CO3** Analyze the various types of waveform generators, timers and data converters. (Analyze)

**CO4** Design amplifiers, oscillators, D-A converters using operational amplifiers. (Create )

**CO5** Design filters using op-amp for a given specification (Apply)

**CO6** Analyze the performance of filters, multivibrators and A/D converter using SPICE. (Analyze)

### **TEXT BOOKS:**

1. D.Roy Choudhry, Shail Jain, —Linear Integrated Circuits, New Age International Pvt. Ltd., 2018, Fifth Edition.
2. Sergio Franco, —Design with Operational Amplifiers and Analog Integrated Circuits, 4th Edition, Tata Mc Graw-Hill, 2016

### **REFERENCE BOOKS:**

1. Ramakant A. Gayakwad, —OP-AMP and Linear ICs, 4th Edition, Prentice Hall / Pearson Education, 2015.
2. S.Salivahanan & V.S. Kanchana Bhaskaran, —Linear Integrated Circuits, TMH,2nd Edition, 4 th Reprint, 2016.
3. Gray and Meyer, —Analysis and Design of Analog Integrated Circuits, Wiley International,5th Edition 2009

# 21UEC404 - LINEAR INTEGRATED CIRCUITS

## UNIT I INTEGRATED CIRCUITS

### **Integrated Circuits :**

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

### **Classification of ICs (Integrated Circuits)**

Below is the classification of **different types of ICs** basis on their chip size.

- **SSI:** Small scale integration. 3 – 30 gates per chip.
- **MSI:** Medium scale integration. 30 – 300 gates per chip.
- **LSI:** Large scale integration. 300 – 3,000 gates per chip.
- **VLSI:** Very large scale integration. More than 3,000 gates per chip.

### **Types of ICs (Integrated Circuits)**

Based on the method or techniques used in manufacturing them, *types of ICs* can be divided into three classes:

1. Thin and thick film ICs
2. Monolithic ICs
3. Hybrid or multichip ICs

Below is the simple explanation of different types of ICs as mentioned above.

#### **Thin and Thick ICs:**

In thin or thick film ICs, passive components such as resistors, capacitors are integrated but the diodes and transistors are connected as separate components to form a single and a complete circuit. Thin and thick ICs that are produced commercially are merely the combination of integrated and discrete (separate) components.

#### **Monolithic ICs**

In monolithic ICs, the discrete components, the active and the passive and also the interconnections between them are formed on a silicon chip. The word monolithic is actually derived from two Greek words “mono” meaning one or single and Lithos meaning stone. Thus monolithic circuit is a circuit that is built into a single crystal.

## Hybrid or Multi chip ICs

As the name implies, “Multi”, more than one individual chips are interconnected. The active components that are contained in this kind of ICs are diffused transistors or diodes. The passive components are the diffused resistors or capacitors on a single chip

## Advantages of ICs

ICs have advantages over those that are made by interconnecting discrete components some of which are its small size.

- It is a thousand times smaller than the discrete circuits. It is an all in one (components and the interconnections are on a single silicon chip). It has little weight.
- Its cost of production is also low.
- It is reliable because there is no soldered joints.
- ICs consumes little energy and can easily be replaced when the need arises.
- It can be operated at a very high temperature.

## Applications of ICs

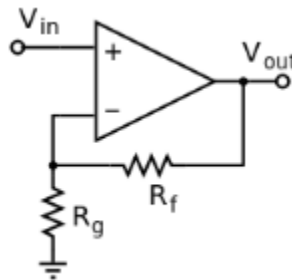
Different types of ICs are widely applied in our electrical devices such as high power amplifiers, voltage regulators, TV receivers and computers etc.

## Operational Amplifier General Conditions

- The Operational Amplifier, or Op-amp as it is most commonly called, can be an ideal amplifier with infinite Gain and Bandwidth when used in the Open-loop mode with typical DC gains of well over 100,000 or 100dB.
- The basic Op-amp construction is of a 3-terminal device, 2-inputs and 1-output, (excluding power connections).
- An Operational Amplifier operates from either a dual positive (+V) and an corresponding negative (-V) supply, or they can operate from a single DC supply voltage.
- The two main laws associated with the operational amplifier are that it has an infinite input impedance, ( $Z = \infty$ ) resulting in “No current flowing into either of its two inputs” and zero input offset voltage “ $V_1 = V_2$ ”.

- An operational amplifier also has zero output impedance, ( $Z = 0$ ).
- Op-amps sense the difference between the voltage signals applied to their two input terminals and then multiply it by some pre-determined Gain, ( $A$ ).
- This Gain, ( $A$ ) is often referred to as the amplifiers “Open-loop Gain”.
- Closing the open loop by connecting a resistive or reactive component between the output and one input terminal of the op-amp greatly reduces and controls this open-loop gain.
- Op-amps can be connected into two basic configurations, Inverting and Non-inverting.

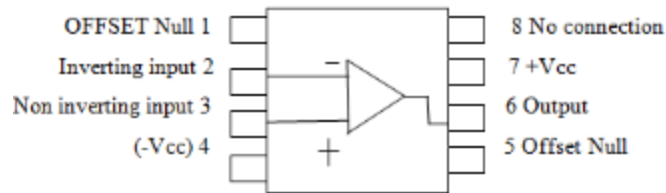
### The Two Basic Operational Amplifier Circuits



- For negative feedback, where the fed-back voltage is in “anti-phase” to the input the overall gain of the amplifier is reduced.
- For positive feedback, where the fed-back voltage is in “Phase” with the input the overall gain of the amplifier is increased.
- By connecting the output directly back to the negative input terminal, 100% feedback is achieved resulting in a Voltage Follower (buffer) circuit with a constant gain of 1 (Unity).
- Changing the fixed feedback resistor ( $R_f$ ) for a Potentiometer, the circuit will have Adjustable Gain.

### Op amp Pin configuration

The pin configuration of op amp is as follows



Where pins 1 and 5 showing Offset Null's along with potentiometer arrangement are used to nullify offset voltages. Positive offsets are nullified with pin 1 and negative offsets are nullified using pin 5. +Vcc and -Vcc are positive and negative supply voltages respectively generally within a range of + or -12 to + or -24.

Pins 2 and 3 are inverting and non inverting input terminals respectively. Maximum differential input voltages will be specified in datasheets which should be exceeded, Opamp may get damaged due to high power dissipation. Pin 6 is single ended output terminal from which output will be taken.

### Characteristics of 741 Opamp

Typical Characteristics of 741 opamp for general purpose at T=25 Deg C,

- Supply voltage around 12 volts
- **Operating temperature** range 0 degrees to 70 degrees for military grade it is -55 to 130 Deg C
- **Vcc** of the range + or -18 with **Output Voltage swing** with load resistance 10 kilo ohms + or -14 volts
- **Maximum power consumption** (dissipated in opamp) around 80 milli watts
- **Slew rate** 0.5 volt/micro second
- **Input Resistance** 2 mega ohms
- **Output resistance** 75 ohms
- **CMRR** (90 db) i.e differential gain/Common mode gain= 31600
- **Offset voltage** 7 milli volts

- **Offset current** 20-200 nano amps maximum
- **Input Bias Current** 80-500 nano amps maximum

### **Ideal Op amp characteristics**

Ideal operational amplifier are characterized by

- Infinite gain
- Infinite input resistance
- Zero output resistance (order of 10's of ohms)
- Infinite bandwidth (practically restricted by slew rate)
- Linear irrespective of entire analog signal range No offsets and, so on

### **Definition of Differential Amplifier**

A differential amplifier is one which amplifies only difference between two signals. Ideally difference amplifier should not amplify signal content common to both input signals. Practically the common mode signal gain will be finite. The efficiency of differential amplifier is quantified in terms of parameter called Common Mode Rejection Ratio. Common Mode Rejection Ratio of an differential amplifier is defined as follows

$$\text{CMMR} = 20 * \log_{10} (A_d/A_c)$$

Where,

**Ad** is differential mode signal gain

**Ac** is common mode signal gain.

### **Need for differential amplifier**

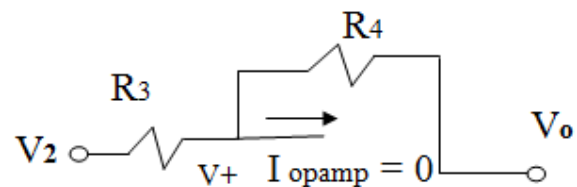
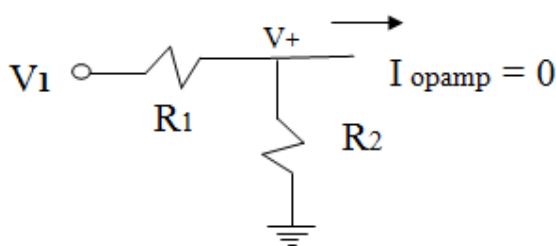
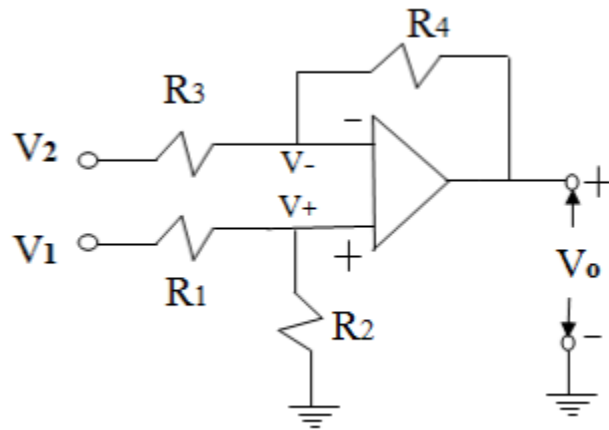
Consider a transducer which provides a small signal at its output terminals which has to be sent to the measuring instrument. The medium carrying these signals for example copper wire may induce an interference signal which is comparable or larger than the transducer output signal. This noise signal is common to both

output terminals. Hence by using differential amplifier at the front end of the amplifier this noise signal can be attenuated to a large extent so that its amplitude is negligible to the transducer output signal.

### Design and Operation of Differential Amplifier

Differential amplifier Design and Operation with circuit diagram:

Consider the simplest design of differential amplifier with one opamp, four resistors R1, R2, R3 and R4. V1 and v2 are the two input voltages applied to non-inverting and inverting terminals of an opamp. In this configuration opamp is given negative feedback hence the concept of **virtual ground** holds and  $V^+ = V^-$ . The above diagram can be simplified and can be redrawn as follows



Due to high input resistance of opamp, it draws no current. Hence

$$V_a = V_1 * \left( \frac{R_2}{R_1 + R_2} \right)$$

Similarly at the non inverting terminal applying Kirchhoff's current law

$$\frac{V_a - V_o}{R_4} + \frac{V_a - V_2}{R_3} = 0$$

$$V_a * \left( \left( \frac{1}{R_3} \right) + \left( \frac{1}{R_4} \right) \right) - \frac{V_o}{R_4} - \frac{V_2}{R_3} = 0$$

$$V_a * \left( \frac{R_3 + R_4}{R_3 * R_4} \right) = \left( \frac{V_o}{R_4} \right) + \left( \frac{V_2}{R_3} \right)$$

Substituting for  $V_a$  from Equation 1 into equation 2

$$V_1 * \left( \frac{R_2}{R_1 + R_2} \right) * \left( \frac{R_3 + R_4}{R_3 * R_4} \right) = \left( \frac{V_o}{R_4} \right) + \left( \frac{V_2}{R_3} \right)$$

$$V_o = V_1 * \left( 1 + \frac{R_4}{R_3} \right) * \frac{1}{1 + \frac{R_1}{R_2}} - V_2 * \left( \frac{R_4}{R_3} \right)$$

From the equations it is evident that for the output to be of the form  $A_d * (V_1 - V_2)$

$$\left( 1 + \frac{R_4}{R_3} \right) * \frac{1}{1 + \frac{R_1}{R_2}} = \left( \frac{R_4}{R_3} \right)$$

Solving further and rearranging terms

$$\left( 1 + \frac{R_3}{R_4} \right) = \left( 1 + \frac{R_1}{R_2} \right)$$

Therefore for the above configuration to work as differential amplifier

$$\frac{R_3}{R_4} = \frac{R_1}{R_2}$$

where differential gain

$$A_d = \left( \frac{R_4}{R_3} \right) = \frac{R_2}{R_1}$$

## Common Mode Gain of Differential Amplifier

Assume that the resistors are not perfectly matched and let  $V_1 = V_{1d} + V_n$  and  $V_2 = V_{2d} + V_n$  where differential input signal is  $V_d = V_{1d} - V_{2d}$  and  $V_n$  is the common input signal. From equation 3 by substituting equations for  $V_1$  and  $V_2$  we get

$$V_0 = V_{1d} * \left(1 + \frac{R_3}{R_4}\right) * \frac{1}{1 + \frac{R_1}{R_2}} - V_{2d} * \left(\frac{R_4}{R_3}\right) + V_n \left( \left(1 + \frac{R_3}{R_4}\right) * \frac{1}{1 + \frac{R_1}{R_2}} - \left(\frac{R_4}{R_3}\right) \right)$$

$$A_c = \left(\frac{R_4}{R_3}\right) \left( \left( \frac{1 + \frac{R_4}{R_3}}{1 + \frac{R_1}{R_2}} \right) - 1 \right)$$

## Disadvantages of Differential Amplifier

1. If the Resistors are selected in such a way that the differential gain of amplifier is high ( $R_1$  is selected to have less value compared to  $R_2$ ) then the input resistance of the amplifier will be less.
2. It is difficult to manipulate differential gain since if we change resistance in one branch then we need to change resistance in other branch so that the condition is satisfied.

## Slew rate of op amp

It is the maximum rate at which output can change in an opamp. It is one of the major limitations in an opamp. It is expressed in volt/second. The output gets distorted if the rate at which output changes exceeds slew rate.

Consider a opamp with slew rate specified in manufacturers datasheet as 10 v/microsecond if we apply a sine wave with frequency  $w$  and amplitude  $A$  maximum product  $A * W * \text{gain}$  can be at most 10v/microsecond before opamp input output characteristics steps into nonlinear regime.

## CMRR of op amp

CMRR is acronym for Common Mode Rejection Ration which is used to quantify how good a differential amplifier is. Let  $V_1 = V_{1d} + V_n$  and  $V_2 = V_{2d} + V_n$

where differential input signal is  $V_d = V_{1d} - V_{2d}$  and  $V_n$  is the common input signal. The output of differential amplifier will be of the form  $V_o = A_d * (V_d) + A_c * V_n$ , then the Common Mode Rejection Ratio of an differential amplifier is defined as the

$$\text{CMMR} = 20 * \log_{10}(A_d/A_c)$$

Where  $A_d$  is differential mode signal gain and  $A_c$  is common mode signal gain.

## DC CHARACTERISTICS

### Input bias current of op amp

Input bias current is defined as average of currents entering the input terminals of an Opamp. Typically these currents are of the order of nano amperes. Let  $I_1$  and  $I_2$  be the currents entering the input terminals of an Opamp the input bias current is given by

$$I_b = (I_1 + I_2) / 2$$

### Inputs offset currents of op amp

Offset current is defined as difference of bias currents entering the input terminals of an Opamp. Typically these currents are of the order of nano amperes. Let  $I_1$  and  $I_2$  be the currents entering the input terminals of an Opamp the input bias current is given by

$$I_f = (I_1 - I_2)$$

### Input offset voltage of opamp

Input offset voltage is the voltage applied at the input terminals of an Opamp to make output zero, typically of the order of milli volts.

### Output offset voltage of opamp

Output offset voltage is defined as Opamp output voltage when both the input terminal voltages of the Opamp are grounded. Universal balancing techniques with potentiometers are often used to balance offset voltages.

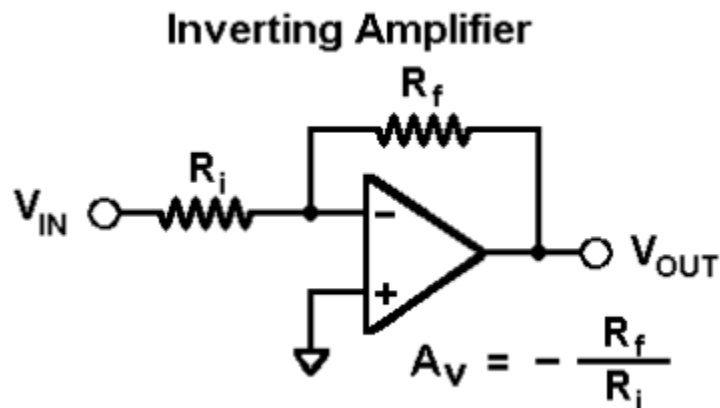
## Inverting amplifier

### Definition

Inverting amplifier is one in which the output is exactly  $180^\circ$  out of phase with respect to input (i.e. if you apply a positive voltage, output will be negative). Output is an inverted (in terms of phase) amplified version of input.

### Circuit operation

The inverting amplifier using opamp is shown in the figure below



Assuming the opamp is ideal and applying the concept of virtual short at the input terminals of opamp, the voltage at the inverting terminal is equal to non inverting terminal. The simplified circuit is shown in the figure below

Applying KCL at inverting node we get

$$(0 - V_i)/R_i + (0 - V_o)/R_f = 0$$

By rearranging the terms we will get

$$\text{Voltage gain } A_V = V_o / V_i = -R_f / R_i .$$

### Gain

Gain of inverting amplifier  $A_V = -R_f / R_i$ .

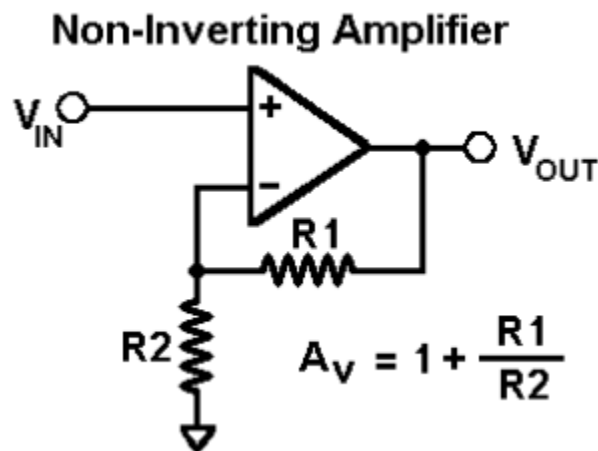
## Non Inverting amplifier

### Definition

Non Inverting amplifier is one in which the output is in phase with respect to input(i.e. if you apply a positive voltage, output will be positive ). Output is an Non inverted(in terms of phase) amplified version of input.

### Circuit operation

The inverting amplifier using opamp is shown in the figure below



Assuming the opamp is ideal and applying the concept of virtual short, the voltage at the inverting terminal is equal to non inverting terminal. Applying KCL at inverting node we get

$$(V_i - V_o)/R_2 + (V_o - 0)/R_1 = 0$$

By rearranging the terms we will get

$$\text{Voltage gain } A_v = V_o / V_i = (1 + R_f / R_i)$$

### Gain

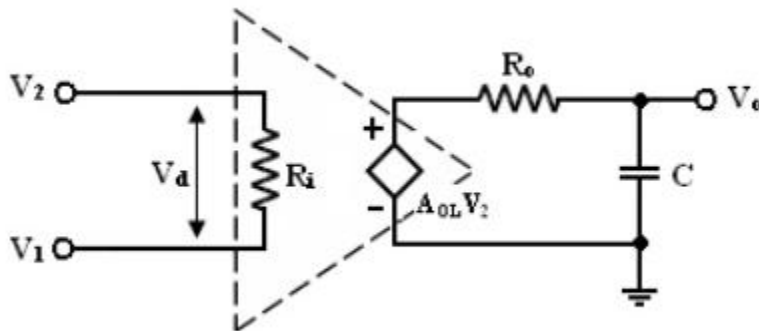
Gain of non inverting amplifier  $A_v = (1 + R_f / R_i)$ .

## AC CHARACTERISTICS:

For small signal sinusoidal (AC) application one has to know the ac characteristics such as frequency response and slew-rate.

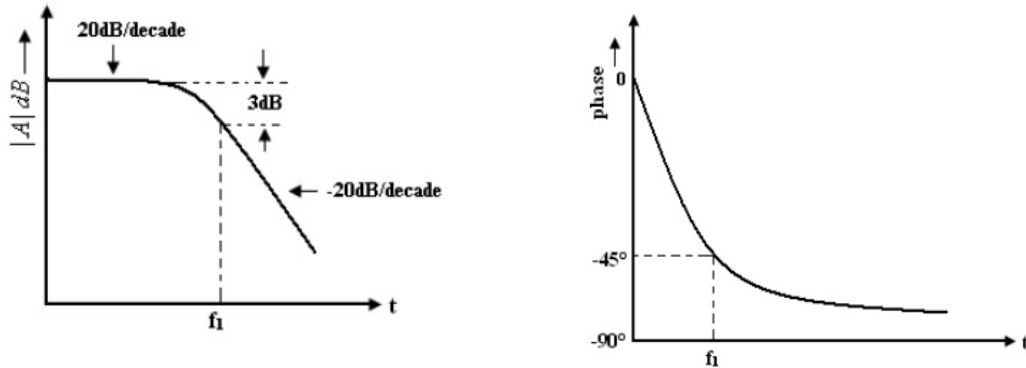
### Frequency Response:

The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response. Op-amp should have an infinite bandwidth  $Bw = \infty$  (i.e) if its open loop gain is 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency. The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.



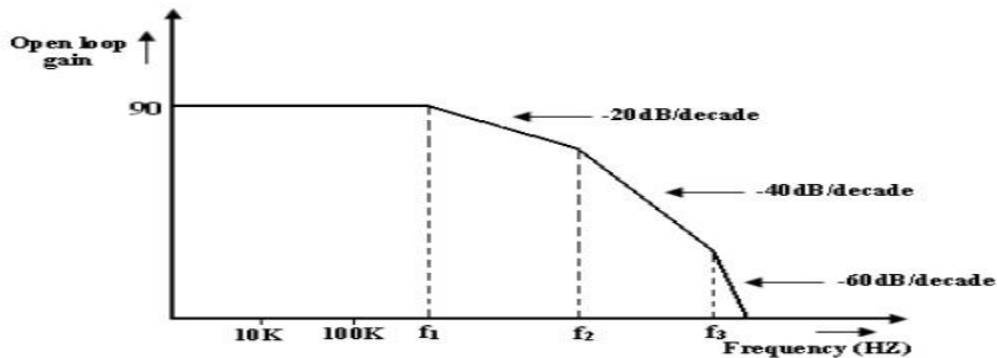
There is one pole due to  $R_o C$  and one  $-20\text{dB/decade}$ . The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.  $f_1$  is the corner frequency or the upper 3 dB frequency of the op-amp. The magnitude and phase angle of the open loop voltage gain are functions of frequency can be written as, The magnitude and phase angle characteristics from eqn (29) and (30) 1. For frequency  $f \ll f_1$  the magnitude of the gain is  $20 \log A_{OL}$  in dB.

- At frequency  $f = f_1$  the gain is 3 dB down from the dc value of AOL in dB. This frequency  $f_1$  is called corner frequency.
- For  $f \gg f_1$  the gain rolls off at the rate of  $-20\text{dB/decade}$  or  $-6\text{dB/decade}$ .



From the phase characteristics that the phase angle is zero at frequency  $f = 0$ .

At the corner frequency  $f_1$  the phase angle is  $-45^\circ$  (lagging) and at infinite frequency the phase angle is  $-90^\circ$ . It shows that a maximum of  $90^\circ$  phase change can occur in an op-amp with a single capacitor  $C$ . Zero frequency is taken as one decade below the corner frequency and infinite frequency is one decade above the corner frequency.



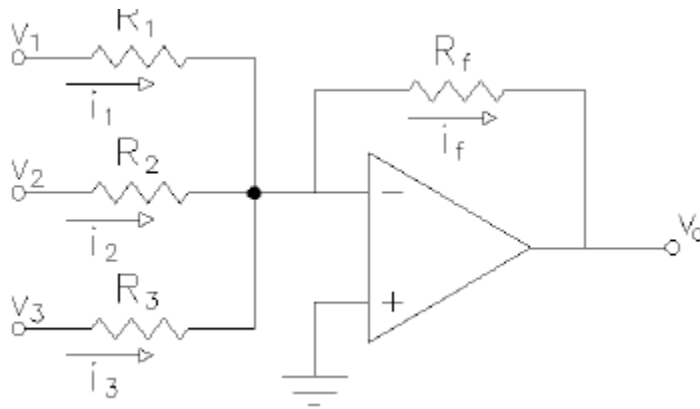
## UNIT II

### OP-AMP APPLICATIONS

#### Summer

The inverting amplifier can also be used as a summing amplifier; that is, it can be made to add the effects of several input voltages together. Look at the circuit in

Fig..



$$i_f = i_1 + i_2 + i_3$$

$$i_f = -\frac{V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$V_o = -\frac{R_f}{R_1}V_1 - \frac{R_f}{R_2}V_2 - \frac{R_f}{R_3}V_3$$

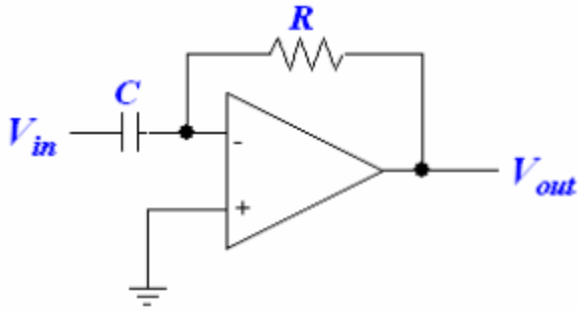
#### Opamp differentiator circuit

##### Definition

Opamp Differentiator is a circuit which provides output proportional to the differential of input signal. If  $V_i$  is the input signal applied to a differentiator then the output is  $V_o = K \cdot dV_o/dt$  where  $K$  is proportionality constant.

Opamp differentiator operation

The opamp differentiator is as shown below



It is obvious from the circuit shown above that negative feedback is provided from output to inverting terminal. Using the concept of virtual ground the inverting terminal will be at zero potential (Since the non inverting terminal of opamp is at ground potential). The differentiator circuit can be redrawn as follows. Applying KCL at inverting node of opamp, we get

$$(0 - V_{out})/R + I_c = 0$$

$$I_c = V_{out}/R$$

where  $I_c = C \cdot d(0 - V_{in})/dt$ . Hence we get  $V_{out} = -R \cdot C \cdot dV_{in}/dt$ .

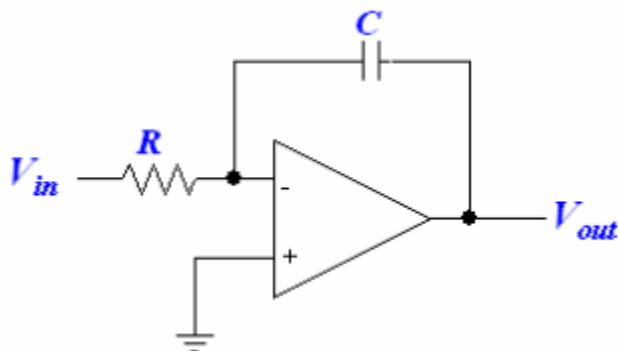
If we apply a periodic triangular signal to opamp differentiator the output will be a periodic square wave.

### Opamp integrator circuit

Integrator is a circuit which provides output proportional to the integral of input signal. If  $V_i$  is the input signal applied to an integrator then the output is  $V_o$  where  $K$  is proportionality constant.

### Opamp integrator operation

The opamp integrator is as shown below



It is obvious from the circuit shown above that negative feedback is provided from output to inverting terminal. Using the concept of virtual ground the inverting terminal will be at zero potential (Since the non inverting terminal of opamp is at ground potential). the integrator circuit can be redrawn as follows  
Applying KCL at inverting node of opamp, we get

$$(0 - V_{out})/R + I_c = 0$$

$$I_c = V_{out}/R$$

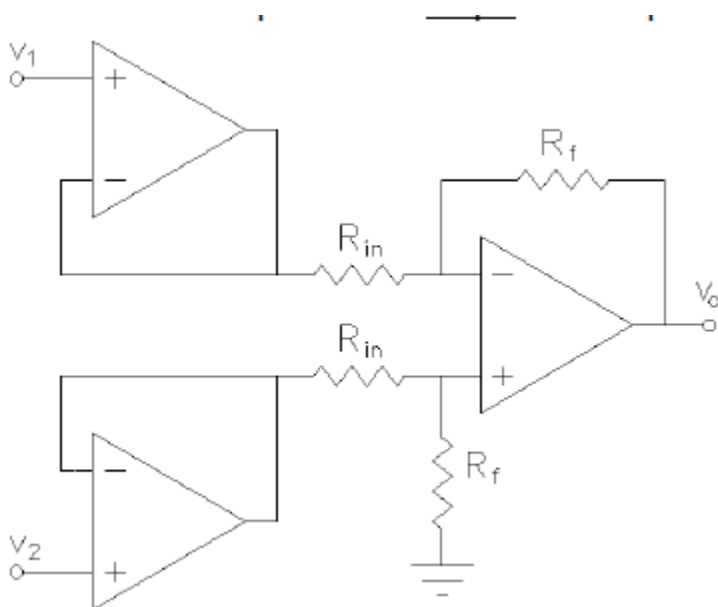
where  $I_c = (-1/C) * \int V_{in} * dt$ . Hence we get

$$V_{out} = - (1/R * C) * \int V_{in} * dt$$

If we apply a period square signal to opamp differentiator the output will be a periodic triangular wave.

### Instrumentation Amplifier

The differential amplifier isn't really very practical. The current that flows into the top input depends on the voltage applied to the bottom input. This may not seem that bad, but it is. It means that the input characteristics of this circuit are not constant. One way to get around this would be to place a voltage follower on each input, as shown here.



$$V_o = \frac{R_f}{R_{in}}(V_2 - V_1)$$

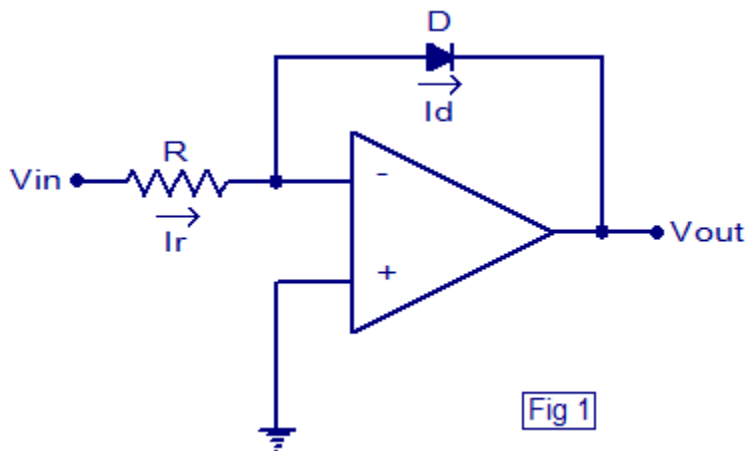
## LOGARITHMIC AMPLIFIER

### Definition

Logarithmic amplifier gives the output proportional to the logarithm of input signal. If  $V_i$  is the input signal applied to a differentiator then the output is  $V_o = K \ln(V_i) + I$  where  $K$  is gain of logarithmic amplifier,  $I$  is constant.

### Logarithmic amplifier operation

The circuit diagram of logarithmic amplifier is as shown below



It is obvious from the circuit shown above that negative feedback is provided from output to inverting terminal. Using the concept of virtual short between the input terminals of an opamp the voltage at inverting terminal will be zero volts. (Since the non inverting terminal of opamp is at ground potential). The logarithmic circuit can be redrawn as follows

The current equation of diode is given as  $I_d = I_{do} * (\exp(V/V_t) - 1)$  where  $I_{do}$  is reverse saturation current,

$V$  is voltage applied across diode;  $V_t$  is the voltage equivalent of temperature. Hence applying KCL at inverting terminal of opamp, we get

$$(0 - V_{in})/R_1 + I_d = 0 \text{ implies } I_d = V_{in}/R_1$$

Substituting the equation for current in the above equation we get  $I_{do} * (\exp(V/V_t) - 1) = V_{in}/R_1$ . Assuming  $\exp(V/V_t) \gg 1$  i.e.  $V \gg V_t$  and  $V = -V_o$ , we get  $I_{do} * \exp(-V_o/V_t) = V_{in}/R_1$ . Applying Antilog on both sides we get

$$V_o = -V_t * \ln(V_{in}/(R_1 * I_{do})).$$

### Gain of logarithmic amplifier

Gain of amplifier  $K = -V_t$

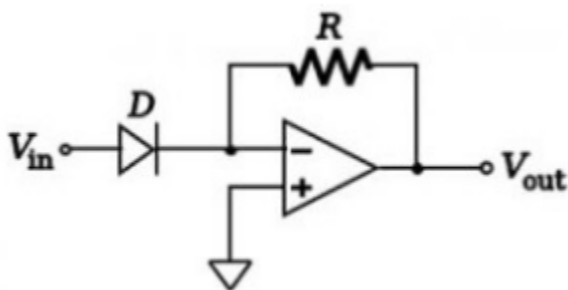
### ANTI LOG AMPLIFIER

#### Definition

Anti log amplifier is one which provides output proportional to the anti log i.e. exponential to the input voltage. If  $V_i$  is the input signal applied to a Anti log amplifier then the output is  $V_o = K * \exp(a * V_i)$  where  $K$  is proportionality constant,  $a$  is constant.

#### Anti log amplifier operation

A simple Anti log amplifier is shown below



It is obvious from the circuit shown above that negative feedback is provided from output to inverting terminal. Using the concept of virtual short between the input terminals of an opamp the voltage at inverting terminal will be zero volts. (Since the non inverting terminal of opamp is at ground potential). The anti log amplifier can be redrawn as follows

The current equation of diode is given as  $I_d = I_{do} * (\exp (V/V_t) - 1)$  where  $I_{do}$  is reverse saturation current,  $V$  is voltage applied across diode;  $V_t$  is the voltage equivalent of temperature

Applying KCL at inverting node of opamp we get

$$I_d = (0 - V_o) / R = I_o * (\exp (V_{in} / V_t)) \text{ (assumed } V_{in} / V_t \gg 1)$$

Hence  $V_o = -I_o * R * (\exp (V_{in} / V_t))$ .

### **Gain of Anti log amplifier**

Gain of Anti log amplifier  **$K = -I_o * R$**

## **SCHMITT TRIGGER**

### **Definition**

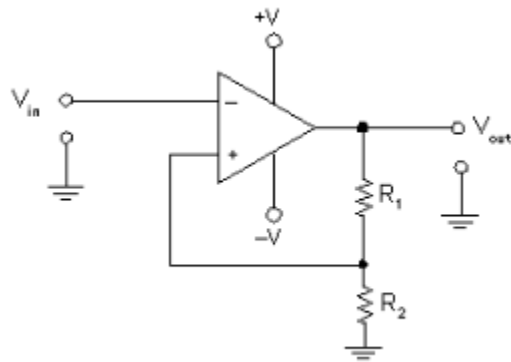
Schmitt trigger is an electronic circuit with positive feedback which holds the output level till the input signal to comparator is higher than the threshold. It converts a sinusoidal or any analog signal to digital signal. It exhibits hysteresis by which the output transition from high to low and low to high will occur at different thresholds.

### **Principle of operation**

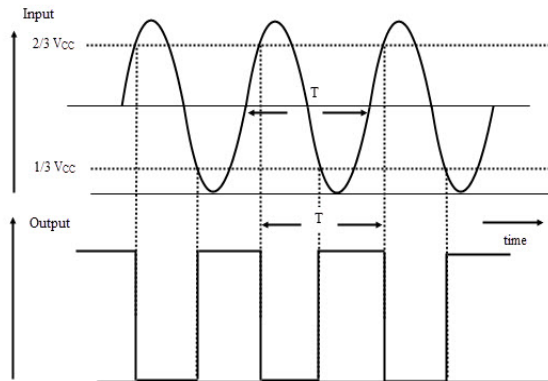
Consider a feedback system with forward gain of **A** and feedback factor **β**. If we adjust the loop gain to be one then the gain with feedback becomes infinite. This results in ever ending transition of output between extremes of output. Schmitt trigger is one of such regenerative circuits also called as astable multivibrator

because of two quasi stable (unstable) states which are 1.positive extreme and 2.negative extreme.

### Circuit diagram



The opamp Schmitt trigger is as shown below



It is obvious from the circuit that positive feedback is employed in the circuit. The feedback factor

$$\beta = V_f / V_o = R_2 / (R_2 + R_1).$$

### Circuit analysis

From the figure shown above let us assume a sinusoidal voltage is applied and at first output is in positive saturation state. Then the feedback voltage  $V_f = \beta * V_{cc}$ . Now when input  $V_{in}$  falls below  $\beta * V_{cc}$  then the voltage at inverting terminal is greater than the voltage at non inverting terminal, so the output will be positive and is equal to  $-V_{cc}$ . This value of input voltage at which output makes transition from positive saturation voltage to negative saturation voltage is called **upper threshold**.

At this point  $V_f = -\beta * V_{cc}$  now if input is allowed to fall below  $-\beta * V_{cc}$  then the voltage at non inverting terminal is greater than the voltage at inverting terminal, so the output makes transition from  $-V_{cc}$  to  $+V_{cc}$ . This value of input voltage at which output makes transition from negative saturation voltage to positive saturation voltage is called **lower threshold**. This process continues till sine wave

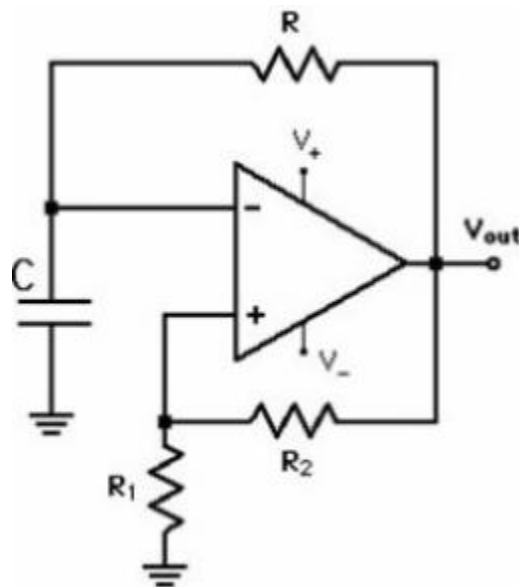
input exists at input and DC power supply for opamp is on. Below is a diagram showing the input and output characteristics of opamp schmitt trigger

## Astable Multivibrator

### Definition

Astable Multivibrator is also called as Free running multivibrator or relaxation oscillator with no stable states. It is a square wave generator and has two unstable states. It oscillates back and forth between these two states when the circuit is given power supply.

### Circuit Diagram



### Design equations

The Time period of Square wave

$$T = 2 * R * C * \ln\left(\frac{1 + \beta}{1 - \beta}\right)$$

Assume  $R_1=R_2$  then  $T= R*C*\ln(3)$ , in which the values of  $R$  and  $C$  can have any combination based on availability of capacitor and resistor but should satisfy the time period equation.

### Circuit analysis

The output of opamp is  $+V_{cc}$  if  $V_2 \gg V_1$  and is  $-V_{cc}$  if  $V_2 \ll V_1$ . Assume that the output initially is at positive saturation value of  $+V_{cc}$ . By voltage divider rule the voltage at non inverting terminal of opamp is  $V_{cc}*R_1/(R_2+R_1)$ . The capacitor starts charging through  $R$  with time constant  $R*C$  and the voltage across capacitor is given by  $V_c = V_{cc}*(1-\exp(-R*C*t))$ . When the voltage across the capacitor is just more than  $V_{cc}*R_1/(R_2+R_1)$ , at that instant the output of opamp changes to  $-V_{cc}$ . Now the  $V_c = -V_{cc}*R_1/(R_2+R_1)$ , the capacitor has to discharge through  $R$  till it reaches to a value less than  $-V_{cc}*R_1/(R_2+R_1)$ . At that instant when  $V_1 \ll -V_{cc}*R_1/(R_2+R_1)$ , output will be  $+V_{cc}$ . During the charging and discharging time voltage across the capacitor will be  $V_c = -V_{cc}*\exp(-R*C*t)$ . Hence the voltage across capacitor switches between  $-V_{cc}*R_1/(R_2+R_1)$  and  $+V_{cc}*R_1/(R_2+R_1)$  and output switches between  $+V_{cc}$  and  $-V_{cc}$ . The voltage across the capacitor during charging time is given by  $V_c = V_{cc}*(1-(1+\beta)\exp(-t/(R*C)))$  where  $\beta = R_1/(R_2+R_1)$ .

Let us assume that the voltage across capacitor at  $t= 0$  s is equal to  $-V_{cc}$ . At  $T/2$  output transits from  $-V_{cc}$  to  $+V_{cc}$ .

Hence at  $t=T/2$   $V_c = \beta*V_{cc}$ , substituting in  $V_c = V_{cc}*(1-(1+\beta)\exp(-t/(R*C)))$  we get

$$\beta*V_{cc} = V_{cc}*(1-(1+\beta)\exp(-T/(2*R*C)))$$

$$T = 2*R*C*\ln((1+\beta)/(1-\beta))$$

Hence the frequency of oscillation of square wave is  $f=1/T$ .

### Remarks

This circuit can be used for generating square waves with frequencies of the Kilo hertz order. The slew rate of opamp poses a limitation in generating still higher frequency square waves.

## UNIT III

### TIMERS & PHASE LOCKED LOOPS

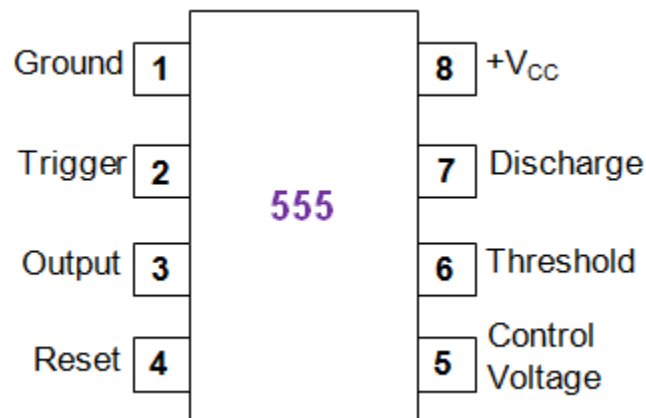
#### INTRODUCTION

It is basically a monolithic timing circuit that produces accurate and highly stable time delays or oscillation. When compared to the applications of an op-amp in the same areas, the 555IC is also equally reliable and is cheap in cost. Apart from its applications as a monostable multivibrator and astable multivibrator, a 555 timer can also be used in dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control devices, voltage regulators etc. The timer IC is setup to work in either of the two modes – one-shot or monostable or as a free-running or astable multivibrator. The SE 555 can be used for temperature ranges between  $-55^{\circ}\text{C}$  to  $125^{\circ}$ . The NE 555 can be used for a temperature range between  $0^{\circ}$  to  $70^{\circ}\text{C}$ .

#### The important features of the 555 timer are :

- It operates from a wide range of power supplies ranging from + 5 Volts to + 18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilo hertz.
- The output of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005 %/  $^{\circ}\text{C}$ .
- The duty cycle of the timer is adjustable.
- The maximum power dissipation per package is 600 mW and its trigger and reset inputs has logic compatibility. More features are listed in the datasheet.

# IC Pin Configuration



- Following is a brief description on the function associated with each of its pins
- Ground (Pin 1 of 8-pin and Pin 3 of 14-pin package): Used as a reference with which each of the voltages is measured.
- Trigger (Pin 2 of 8-pin and Pin 4 of 14-pin package): This pin is used to provide trigger to the circuit when the device will be configured to behave like a monostable multivibrator. As evident from Figure 2, it is seen that this pin is connected as an input to the comparator C2 which compares it with  $\frac{1}{3} V_{CC}$ , fed as an input to its other terminal. As a result, when the user-provided negative pulse exceeds  $\frac{1}{3} V_{CC}$  (obtained from the resistive network), the output of this comparator goes high. This causes the output Q of the SR flip-flop to become zero, thereby pulling its  $\bar{Q}$  pin high which makes the output of the inverter to go low, thereby resulting in a high output from the IC.
- Output (Pin 3 of 8-pin and Pin 5 of 14-pin package): This is the pin at which the output of the IC can be obtained. 555 timer IC provides two options for the user to load this pin viz., (i) Normally on load configuration where the load is connected between the Supply and the Output pins and (ii) Normally off load configuration where the load is connected between the Ground and the Output pins.

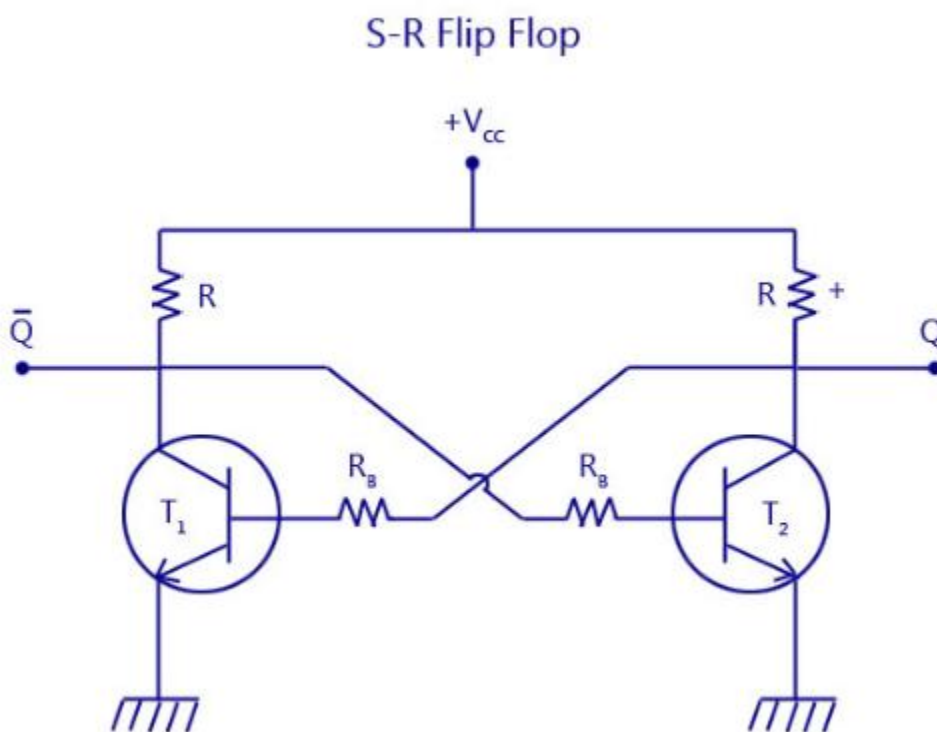
- **Reset** (Pin 4 of 8-pin and Pin 6 of 14-pin package): This pin can be used by the user to reset the IC as the user-provided negative going pulse on this pin switches OFF the associated transistor. This is because, a logic low on this pin causes the output of the flip-flop to go high, turning ON the discharge transistor. However, usually this pin will be connected to +VCC when not in use so as to avoid false triggering.
- **Control Voltage** (Pin 5 of 8-pin and Pin 9 of 14-pin package): This pin is used to control the levels of threshold as well as triggering. In addition, this pin can be used to control the pulse width of the output waveform as the voltage applied at this pin decides the condition at which the output of the comparator (C1) switches its state. The same regulation in the output waveform can be even experienced by connecting a potentiometer to this pin. Next, it is to be noted that when this pin is to be left unused, it is to be bypassed to ground via 0.01  $\mu$ F capacitor in order to get rid of noise issue.
- **Threshold** (Pin 6 of 8-pin and Pin 10 of 14-pin package): This pin is connected to the positive terminal of the comparator C1 which compares the applied voltage with  $\frac{2}{3}$  VCC. Next, when the user provided voltage exceeds this reference level of  $\frac{2}{3}$  VCC, the output of C1 goes high, and thus the flip-flop's output (Q) will be set. Due to this, the complement of its output ( $\bar{Q}$ ) will go low, resulting in a high output from the inverter, which will be nothing but the output of the IC.
- **Discharge** (Pin 7 of 8-pin and Pin 12 of 14-pin package): This pin is connected to the collector terminal of the internal transistor in **555 timer IC**. Generally, a capacitor will be connected between this terminal and ground. This capacitor discharges through the transistor when it saturates, a phenomenon experienced when the output of comparator C1 sets the flip-flop indicating that the threshold voltage has increased in comparison with that of the control voltage. On the other hand, if the negative-going trigger pulse exceeds  $\frac{1}{3}$  VCC, then the output of the flip-flop goes low as the lower comparator's output will go high. This inturn

turns OFF the transistor during which the capacitor attached to its terminal starts to charge at a rate decided by the external resistor and the capacitor.

- Supply (Pin 8 of 8-pin and Pin 13 of 14-pin package): This pin is used to provide a voltage within the range of +5V to +18V wrt ground.

## 555 Timer Basics

- The **555 timer** combines a relaxation oscillator, two comparators, an R-S flip-flop, and a discharge capacitor.



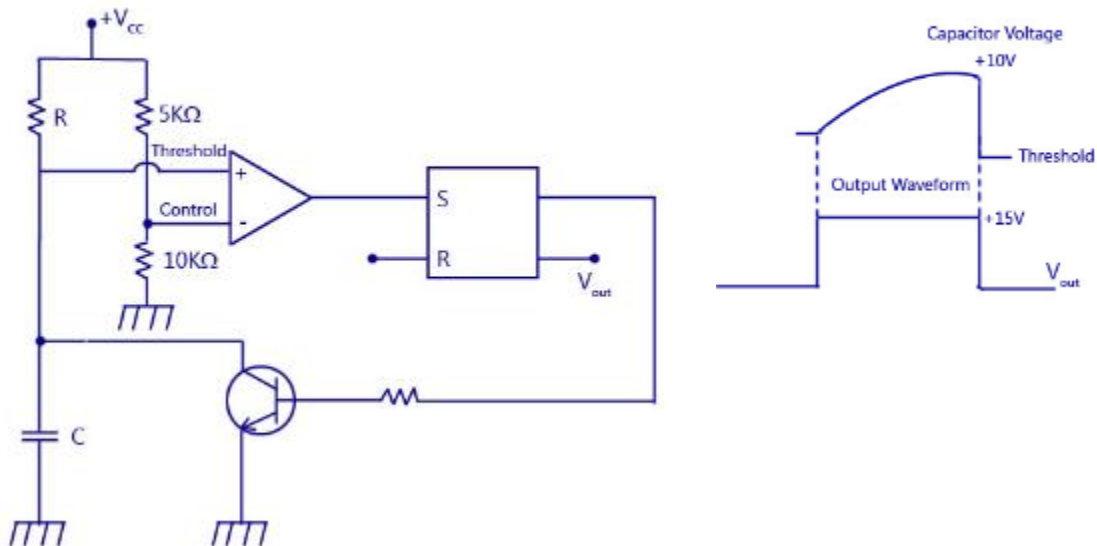
- As shown in the figure, two transistors T<sub>1</sub> and T<sub>2</sub> are cross coupled. The collector of transistor T<sub>1</sub> drives the base of transistor T<sub>2</sub> through the resistor R<sub>b2</sub>. The collector of transistor T<sub>2</sub> drives the base of transistor T<sub>1</sub> through resistor R<sub>b1</sub>. When one of the transistor is in the saturated state, the other transistor will be in the cut-off state. If we consider the transistor T<sub>1</sub> to be saturated, then the collector voltage will be almost zero. Thus there will be a zero base drive for transistor T<sub>2</sub> and will go into cut-off state

and its collector voltage approaches  $+V_{cc}$ . This voltage is applied to the base of T1 and thus will keep it in saturation.

S-R Flip Flop Symbol



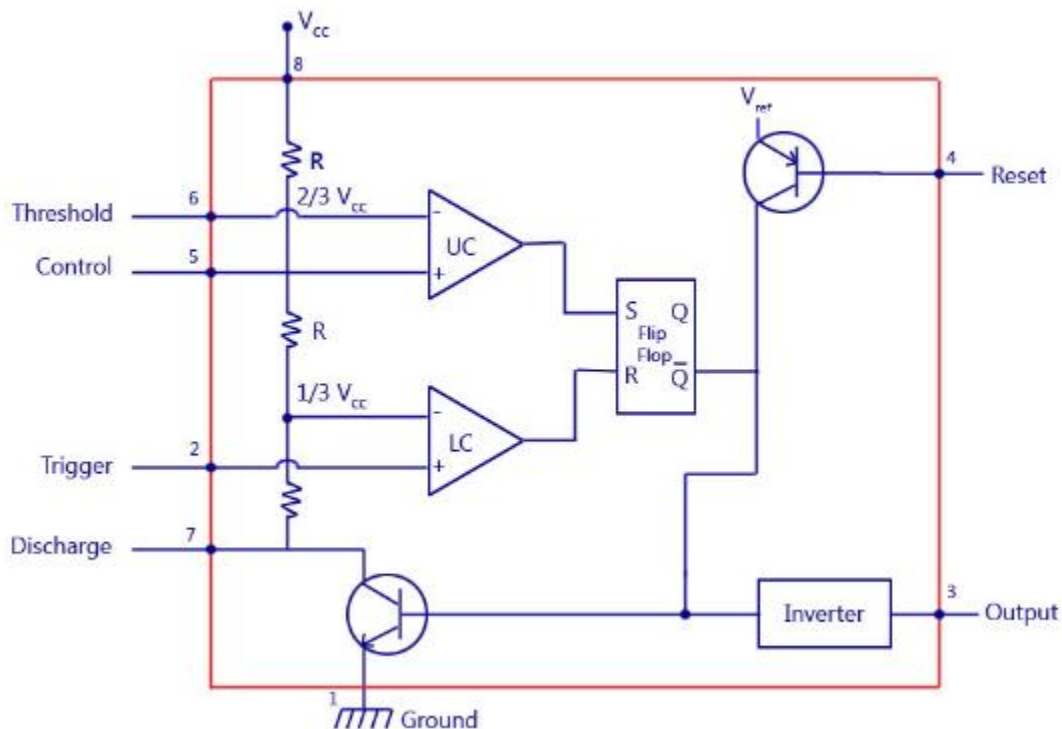
- Now, if we consider the transistor T1 to be in the cut-off state, then the collector voltage of T1 will be equal to  $+V_{cc}$ . This voltage will drive the base of the transistor T2 to saturation. Thus, the saturated collector output of transistor T2 will be almost zero. This value when fed back to the base of the transistor T1 will drive it to cut-off. Thus, the saturation and cut-off value of anyone of the transistors decides the high and low value of Q and its complement. By adding more components to the circuit, an R-S flip-flop is obtained. R-S flip-flop is a circuit that can set the Q output to high or reset it low. Incidentally, a complementary (opposite) output  $\bar{Q}$  is available from the collector of the other transistor. The schematic symbol for a S-R flip flop is also shown above. The circuit latches in either the Q state or its complementary state. A high value of S input sets the value of Q to go high. A high value of R input resets the value of Q to low. Output Q remains in a given state until it is triggered into the opposite state.



## Basic Timing Concept

- From the figure above, assuming the output of the S-R flip flop, Q to be high. This high value is passed on to the base of the transistor, and the transistor gets saturated, thus producing a zero voltage at the collector. The capacitor voltage is clamped at ground, that is, the capacitor C is shorted and cannot charge.
- The inverting input of the comparator is fed with a control voltage, and the non-inverting input is fed with a threshold voltage. With R-S flip flop set, the saturated transistor holds the threshold voltage at zero. The control voltage, however, is fixed at  $\frac{2}{3} V_{CC}$ , that is, at 10 volts, because of the voltage divider.
- Suppose that a high voltage is applied to the R input. This resets the flip-flop R-Output Q goes low and the transistor is cut-off. Capacitor C is now free to charge. As this capacitor C charges, the threshold voltage rises. Eventually, the threshold voltage becomes slightly greater than (+ 10 V). The output of the comparator then goes high, forcing the R S flip-flop to set. The high Q output saturates the transistor, and this quickly discharges the capacitor. An exponential rise is across the capacitor C, and a positive going pulse appears at the output Q. Thus capacitor voltage VC is exponential while the output is rectangular. This is shown in the figure above.

# 555 IC Timer Block Diagram



The block diagram of a **555 timer** is shown in the above figure. A 555 timer has two comparators, which are basically 2 op-amps), an R-S flip-flop, two transistors and a resistive network.

- Resistive network consists of three equal resistors and acts as a voltage divider.
- Comparator 1 compares threshold voltage with a reference voltage +  $2/3 V_{CC}$  volts.
- Comparator 2 compares the trigger voltage with a reference voltage +  $1/3 V_{CC}$  volts.

Output of both the comparators is supplied to the flip-flop. Flip-flop assumes its state according to the output of the two comparators. One of the two transistors is a discharge transistor of which collector is connected to **pin 7**. This transistor saturates or cuts-off according to the output state of the flip-flop. The saturated transistor provides a discharge path to a capacitor connected externally. Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the whole timer irrespective of any input.

## Working Principle

The internal resistors act as a voltage divider network, providing  $(2/3)V_{CC}$  at the non-inverting terminal of the upper comparator and  $(1/3)V_{CC}$  at the inverting terminal of the lower comparator. In most applications, the control input is not used, so that the control voltage equals  $+(2/3)V_{CC}$ . Upper comparator has a threshold input (pin 6) and a control input (pin 5). Output of the upper comparator is applied to set (S) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the upper comparator will set the flip-flop and its output is high. A high output from the flip-flop when given to the base of the discharge transistor saturates it and thus discharges the transistor that is connected externally to the discharge pin 7. The complementary signal out of the flip-flop goes to pin 3, the output. The output available at pin 3 is low. These conditions will prevail until lower comparator triggers the flip-flop. Even if the voltage at the threshold input falls below  $(2/3)V_{CC}$ , that is upper comparator cannot cause the flip-flop to change again. It means that the upper comparator can only force the flip-flop's output high.

To change the output of flip-flop to low, the voltage at the trigger input must fall below  $+(1/3)V_{CC}$ . When this occurs, lower comparator triggers the flip-flop, forcing its output low. The low output from the flip-flop turns the discharge transistor off and forces the power amplifier to output a high. These conditions will continue independent of the voltage on the trigger input. Lower comparator can only cause the flip-flop to output low.

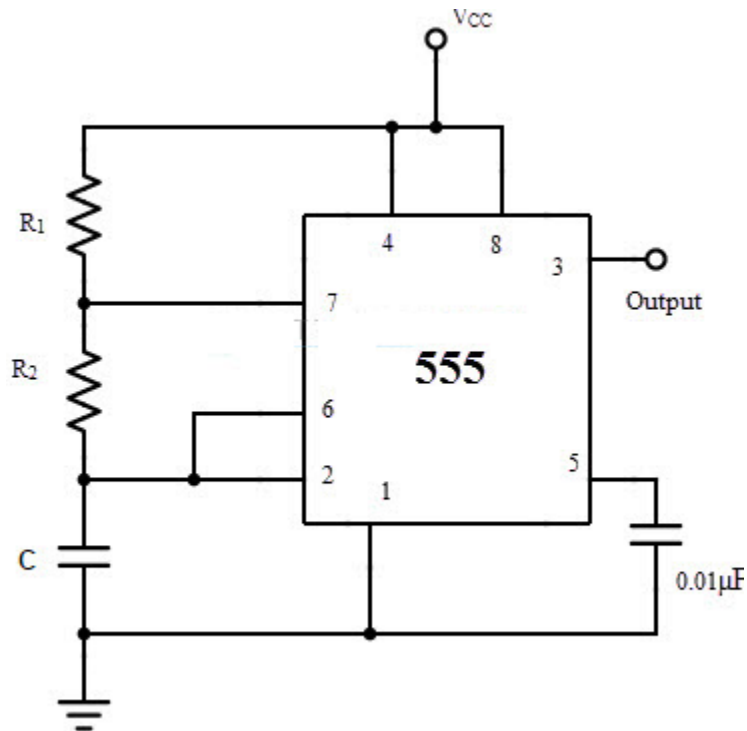
From the above discussion it is concluded that for the having low output from the timer 555, the voltage on the threshold input must exceed the control voltage or  $+(2/3)V_{CC}$ . This also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below  $+(1/3)V_{CC}$ . This turns the discharge transistor off.

A voltage may be applied to the control input to change the levels at which the switching occurs. When not in use, a 0.01 nano Farad capacitor should be connected between pin 5 and ground to prevent noise coupled onto this pin from causing false triggering.

Connecting the reset (pin 4) to a logic low will place a high on the output of flip-flop. The discharge transistor will go on and the power amplifier will output a low.

This condition will continue until reset is taken high. This allows synchronization or resetting of the circuit's operation. When not in use, reset should be tied to +VCC.

### Astable multivibrator using 555 Timer

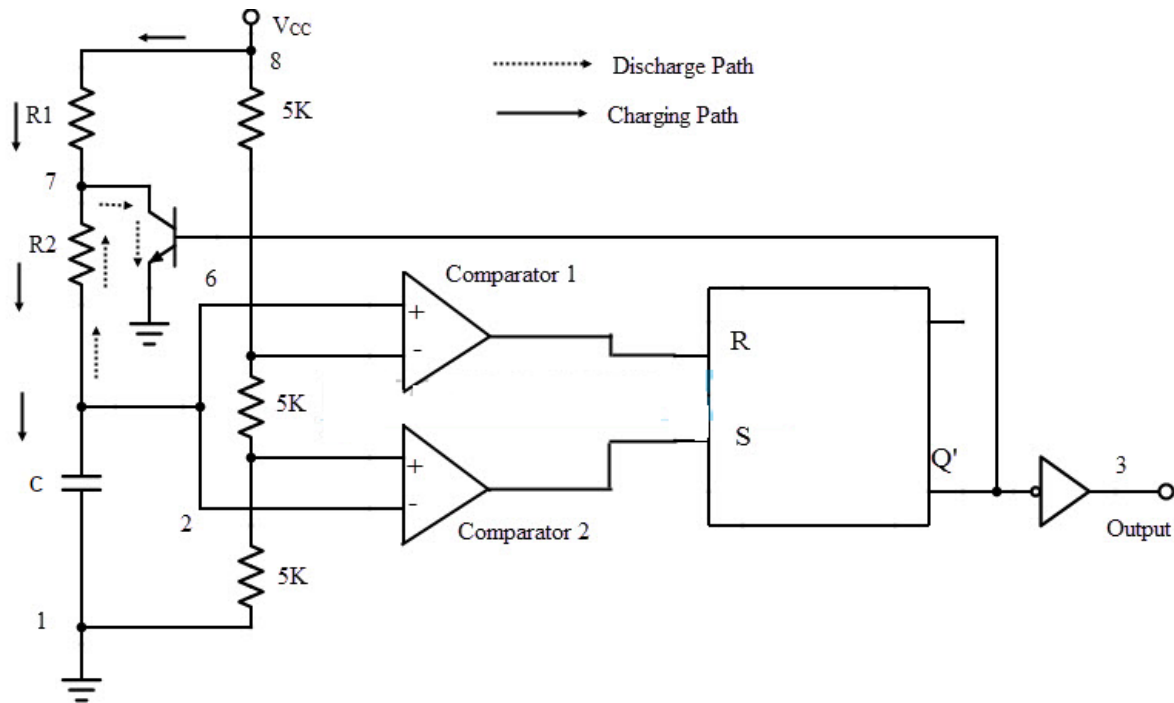


The pins 2 and 6 are connected and hence there is no need for an external trigger pulse. It will self trigger and act as a free running multivibrator. The rest of the connections are as follows: pin 8 is connected to supply voltage (VCC). Pin 3 is the output terminal and hence the output is available at this pin. Pin 4 is the external reset pin. A momentary low on this pin will reset the timer. Hence when not in use, pin 4 is usually tied to VCC.

The control voltage applied at pin 5 will change the threshold voltage level. But for normal use, pin 5 is connected to ground via a capacitor (usually 0.01μF), so the external noise from the terminal is filtered out. Pin 1 is ground terminal. The timing circuit that determines the width of the output pulse is made up of R1, R2 and C.

## Operation

The following schematic depicts the internal circuit of the IC 555 operating in astable mode. The RC timing circuit incorporates R1, R2 and C.



The detailed operation can be explained as follows. Initially, the flip-flop is RESET. This will allow the discharge transistor to go to saturation. The capacitor C, which is connected to the open collector (drain in case of CMOS) of the transistor, is provided with a discharge path. Hence the capacitor discharges completely and the voltage across it is 0. The output at pin 3 is low (0).

When a negative going trigger pulse input is applied to the trigger comparator (comparator 2), it is compared with a reference voltage of  $\frac{1}{3} V_{CC}$ . The output remains low until the trigger input is greater than the reference voltage. The moment trigger voltage goes below  $\frac{1}{3} V_{CC}$ , the output of comparator goes high and this will SET the flip-flop. Hence the output at pin 3 will become high.

At the same time, the discharge transistor is turned OFF and the capacitor C will begin to charge and the voltage across it rises exponentially. This is nothing but the threshold voltage at pin 6. This is given to the comparator 1 along with a

reference voltage of  $2/3 V_{CC}$ . The output at pin 3 will remain HIGH until the voltage across the capacitor reaches  $2/3 V_{CC}$ .

The instance at which the threshold voltage (which is nothing but the voltage across the capacitor) becomes more than the reference voltage, the output of the comparator 1 goes high. This will RESET the flip-flop and hence the output at pin 3 will fall to low (logic 0) i.e. the output returns to its stable state. As the output is low, the discharge transistor is driven to saturation and the capacitor will completely discharge.

Hence it can be noted that the output at pin 3 is low at start, when the trigger becomes less than  $1/3 V_{CC}$  the output at pin 3 goes high and when the threshold voltage is greater than  $2/3 V_{CC}$  the output becomes low until the occurrence of next trigger pulse. A rectangular pulse is produced at the output. The time for which the output stays high or the width of the rectangular pulse is controlled by the timing circuit i.e. the charging time of the capacitor which depends on the time constant  $RC$ .

### ***Pulse Width Derivation***

We know that the voltage across the capacitor  $C$  rises exponentially. Hence the equation for the capacitor voltage  $V_C$  can be written as

$$V_C = V_{CC} (1 - e^{-t/RC})$$

When the capacitor voltage is  $2/3 V_{CC}$ , then

$$2/3 V_{CC} = V_{CC} (1 - e^{-t/RC})$$

$$2/3 = 1 - e^{-t/RC}$$

$$e^{-t/RC} = 1/3$$

$$-t/RC = \ln(1/3)$$

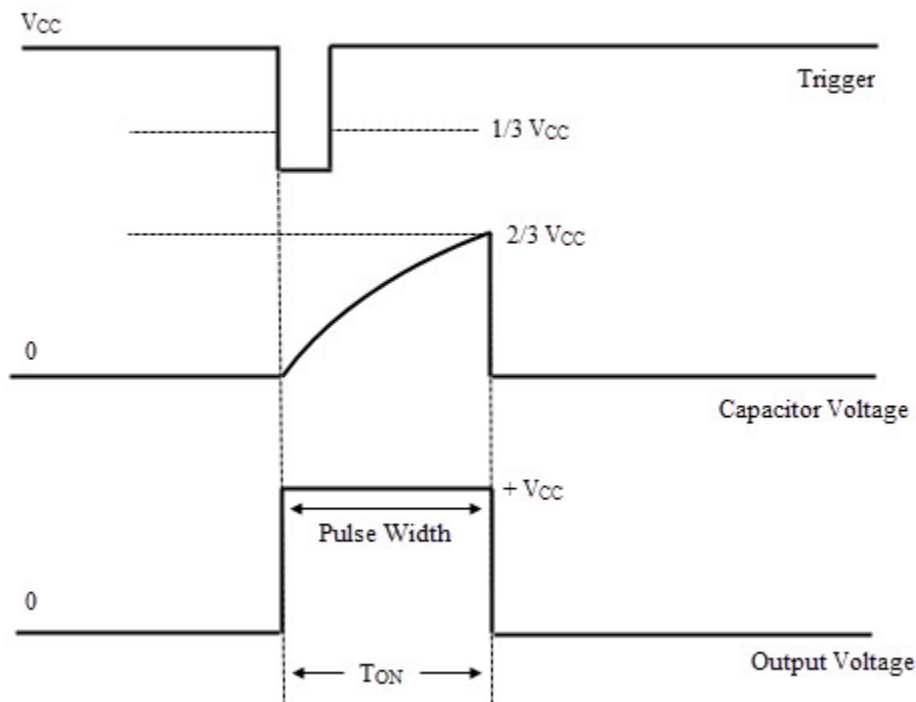
$$-t/RC = -1.098$$

$$t = 1.098 RC$$

$$\therefore t \approx 1.1 RC$$

The pulse width of the output rectangular pulse is  $W = 1.1 RC$ .

The waveforms of the monostable operation are shown below.



## Applications of Monostable Multivibrator

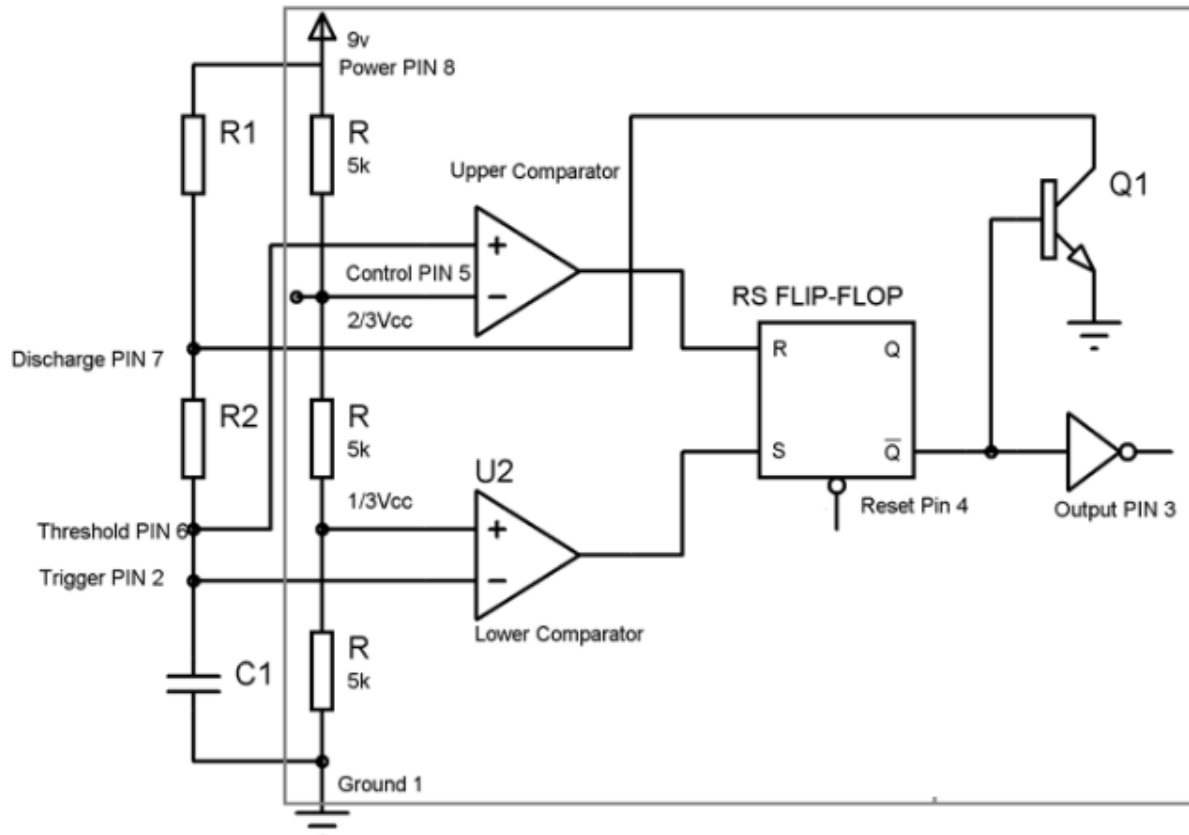
- Frequency Divider
- Pulse Width Modulation
- Linear Ramp Generator
- Missing Pulse Detector

## Astable Multivibrator using 555 Timer IC

Astable Multivibrator mode of 555 timer IC is also called Free running or self-triggering mode. Unlike Monostable Multivibrator mode it doesn't have any stable state, it has two quasi stable state (HIGH and LOW). No external triggering is required in Astable mode, it automatically interchange its two states on a particular interval, hence generates a rectangular waveform. This time duration of

HIGH and LOW output has been determined by the external resistors (R1 and R2) and a capacitor(C1).

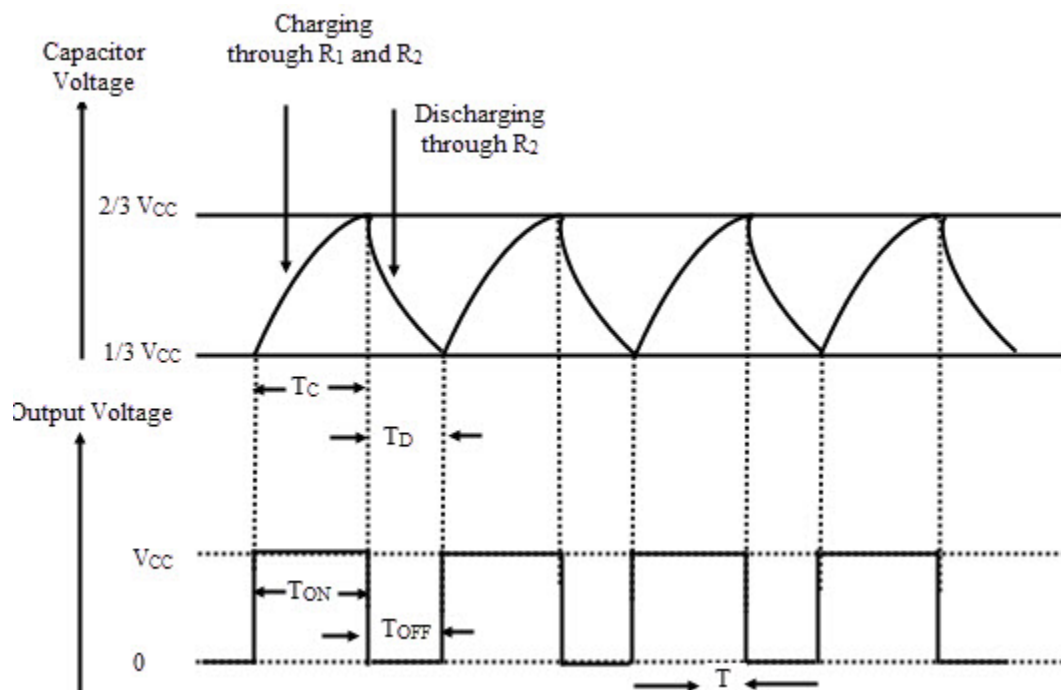
### Operation of Astable Multivibrator mode of 555 timer IC:



- When initially power is turned ON, Trigger Pin voltage is below  $V_{cc}/3$ , that makes the lower comparator output HIGH and SETS the flip flop and output of the 555 chip is HIGH.
- This makes the transistor Q1 OFF, because  $Q_{bar}$ ,  $Q'=0$  is directly applied to base of transistor. As the transistor is OFF, capacitor C1 starts charging and when it gets charged to a voltage above than  $V_{cc}/3$ , then Lower comparator output becomes LOW (Upper comparator is also at LOW) and Flip flop output remains the same as previous (555 output remains HIGH).
- Now when capacitor charging gets to voltage above than  $2/3V_{cc}$ , then the voltage of non-inverting end (Threshold PIN 6) becomes higher than the

inverting end of the comparator. This makes Upper comparator output HIGH and RESETs the Flip flop, output of 555 chip becomes LOW.

- As soon as the output of 555 get LOW means  $Q'=1$ , then transistor Q1 becomes ON and short the capacitor C1 to the Ground. So the capacitor C1 starts discharging to the ground through the Discharge PIN 7 and resistor R2.
- As capacitor voltage get down below the  $2/3 V_{cc}$ , upper comparator output becomes LOW, now SR Flip flop remains in the previous state as both the comparators are LOW.
- While discharging, when capacitor voltage gets down below  $V_{cc}/3$ , this makes the Lower comparator output HIGH (upper comparator remain LOW) and Sets the flip flop again and 555 output becomes HIGH.
- Transistor Q1 becomes OFF and again capacitor C1 starts charging.



This charging and discharging of capacitor continues and a rectangular oscillating output wave for is generated. While capacitor is getting charge the output of 555 is HIGH, and while capacitor is getting discharge output will be LOW. So this is called **Astable mode** because none of the state is stable and 555 automatically interchange its state from HIGH to LOW and LOW to HIGH, so it is called Free running Multivibrator.

Now the OUTPUT HIGH and OUTPUT LOW duration, is determined by the Resistors R1 & R2 and capacitor C1. This can be calculated using below formulas:

$$\text{Time High (Seconds) } T_1 = 0.693 * (R_1 + R_2) * C_1$$

$$\text{Time Low (Seconds) } T_2 = 0.693 * R_2 * C_1$$

$$\text{Time Period } T = \text{Time High} + \text{Time Low} = 0.693 * (R_1 + 2 * R_2) * C_1$$

$$\text{Frequency } f = 1 / \text{Time Period} = 1 / 0.693 * (R_1 + 2 * R_2) * C_1 = 1.44 / (R_1 + 2 * R_2) * C_1$$

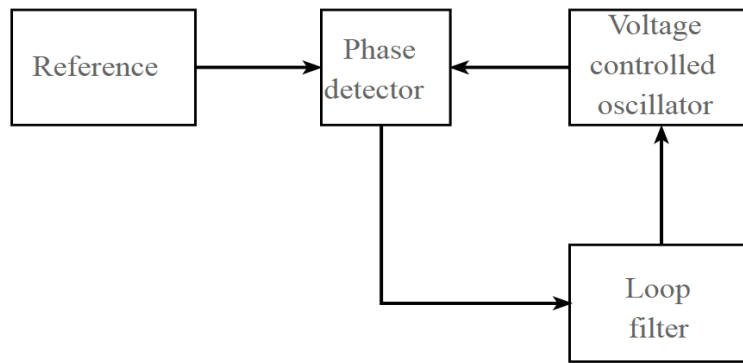
**Duty Cycle:** Duty cycle is the ratio of time for which the output is HIGH to the total time.

$$\text{Duty cycle \%: } (\text{Time HIGH} / \text{Total time}) * 100 = (T_1 / T) * 100 = (R_1 + R_2) / (R_1 + 2 * R_2) * 100$$

Here is the practical demonstration of the **Astable mode of 555 timer IC**, where we have connected a LED to the output of the 555 IC. In this **555 astable multivibrator circuit**, LED will switch ON and OFF automatically with a particular duration. ON time, OFF time, Frequency etc can be calculated using above formulas.

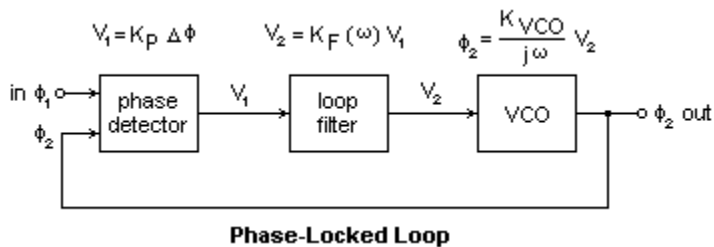
## PHASE LOCKED LOOP

A phase locked loop consist of a phase detector and a voice control oscillator. The output of the phase detector is the input of the voice control oscillator (VCO) and the output of the VCO is connected to one of the inputs of phase detector which is shown below in the basic block diagram. When these two devices are feed to each other the loop forms.



## Block Diagram And Working Principle Of PLL

The phase locked loop consists of a phase detector, a voltage control oscillator and, in between them, a low pass filter is fixed. The input signal 'Vi' with an input frequency 'Fi' is conceded by a phase detector. Basically the phase detector is a comparator which compares the input frequency fi through the feedback frequency fo. The output of the phase detector is (fi+fo) which is a DC voltage. The out of the phase detector, i.e., DC voltage is input to the low pass filter (LPF); it removes the high frequency noise and produces a steady DC level, i.e., Fi-Fo. The Vf is also a dynamic characteristic of the PLL.



The output of the low pass filter, i.e., DC level is passed on to the VCO. The input signal is directly proportional to the output frequency of the VCO (fo). The input and output frequencies are compared and adjusted through the feedback loop until the output frequency is equal to the input frequency. Hence, the PLL works like free running, capture, and phase lock.

When there is no input voltage applied, then it is said to be as a free running stage. As soon as the input frequency applied to the VOC changes and produces an output frequency for comparison, it is called as capture stage. The below figure shows the block diagram of the PLL.

## Phase Locked Loop Detector

The phase locked loop detector compares the input frequency and the output frequency of the VCO to produce a DC voltage which is directly proportional to the phase distinction of the two frequencies. The analog and digital signals are used in the phase locked loop. Most of the monolithic PLL integrated circuits use an analog phase detector and majority of phase detectors are from the digital type. A double balanced mixture circuit is used commonly in analog phase detectors. Some common phase detectors are given below:

### *Exclusive OR Phase Detector*

An exclusive OR phase detector is CMOS IC 4070 type. The input and output frequencies are applied to the EX OR phase detector. To obtain the output high at least one input should be low and the other conditions of output are low which is shown in the below truth table. Let us consider the waveform, the input and output frequencies, i.e.  $f_i$  and  $f_o$  have a phase difference of 0 degrees. Then the DC output voltage of the comparator will be a function of the phase difference between the two inputs.

## PLL Applications

- Frequency Modulation (FM) stereo decoders, FM Demodulation networks for FM operation.
- Frequency synthesis that provides multiple of a reference signal frequency.
- Used in motorspeed controls, tracking filters.
- Used in frequency shift keying (FSK) decodes for demodulation carrier frequencies.