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Department of Electronics and Communication Engineering

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EXPERIENCE	INDUSTRY	TEACHING	TOTAL	
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DATE OF JOININGTHE INSTITUTION	20.06.2011			
RESEARCH FOCUS	***VLSI Testing***			
SUBJECT COMPETENCY				*Digital Signal Processing, VLSI Design, Low power testing*
NO OF JOURNAL PUBLICATION (INTERNATIONAL/NATIONAL)	International - 10			
NO OF CONFERENCE ATTENDED (INTERNATIONAL/NATIONAL)	International – 6 National - 4			
NO OF BOOKS PUBLISHED	-			

Academic Credentials

Level	Degree	Specialization	University	Year of Completion
UG	B.E	ECE	Anna University	2009
PG	M.E	Communication Systems	Anna University	2011

Ph.D	Ph.D	VLSI Testing	Bharath University	2018

Details of Journal Publication:

1. **R Karthick**, M Sundararajan, A Reconfigurable Method for TimeCorrelated Mimo Channels with a Decision Feedback Receiver, International Journal of Applied Engineering Research 12 (15), 5234-52414,2017.

2. **R Karthick**, M Sundararajan , PSO BASED OUT-OF-ORDER (OOO) EXECUTION SCHEME FORHT-MPSOC

,Journal of Advanced Research in Dynamical and Control Systems 9, 1969

3. **R Karthick**, M Sundararajan, Design and Implementation of Low Power Testing Using Advanced Razor Based Processor, ,International Journal of Applied Engineering Research 12 (17), 6384-6390

4. **R Karthick**, M Sundararajan ,A novel 3-D-IC test architecture-a review

,International Journal of Engineering and Technology (UAE) 7 (1.1), 582-586

5. **R Karthick**, P Selvaprasanth, A Manoj Prabaharan,INTEGRATED SYSTEM FOR REGIONAL NAVIGATOR AND SEASONS MANAGEMENT, International Journal of Global Research in Computer Science (UGC Approved …

6. **R Karthick** ,N Sathiyanathan ,MEDICAL IMAGE COMPRESSION USING VIEW COMPENSATED WAVELET TRANSFORM

,Journal of Global Research in Computer Science 9 (9), 01-04

7. R **Karthick**, DM Sundararajan , Fault Tolerant 3D-Integrated Circuits Modeling with an Improved BIST Model

,International journal of printing packaging and allied Sciences 4 (6), 4336-4350

8. **karthick**.R,Hardware Evaluation of Second round SHA-3 Candidates Using FPGA

DRMS International Journal of Advanced Research in Computer Science and …

9. **Karthick**.R,Dr.V.Saminadan Field Programmable Gate Array Implementation of S-R-S-3 Hardware Schema

,international journal of advanced research in computer science and …

10**. Karthick.R** E Shapna Multi-Input - Multi -Output Network systems in DERS using Self-Tuning Proportional Integrative plus Derivative (SPID) Controller

, K R,International Journal of Engineering And Computer Science 2 (7), 2167-2176.